

## ABSTRACT OF THE DISCLOSURE

A margin test on a Dynamic Random Access Memory (DRAM) in accordance with the invention begins with a supply voltage level being stored in all memory cells of the DRAM. Circuitry incorporated into each sense amplifier of the DRAM then isolates the digit line equilibrating circuitry in each sense amplifier from the cell plate voltage DVC2 or supply voltage  $V_{CC}$  to which the equilibrating circuitry is normally connected and connects the equilibrating circuitry to ground instead.

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